A GaAs MULTI-FUNCTION X-BAND MMIC FOR SPACE-BASED SAR APPLICATION WITH 7 BIT PHASE AND AMPLITUDE CONTROL

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ABSTRACT

The design and performance of a low power GaAs multi-function X-band MMIC for space-based synthetic aperture radar (SAR) application with 7 bit phase and amplitude control, is described. The multi-function chip (MFC) consists of switches for selection of the transmit or receive mode, a 7-bit phase shifter, a 7-bit attenuator and several amplifiers. The MFC frequency range is 9 to 11 GHz for both transmit and receive. The phase setting of the MFC is from 0° to 360° with an accuracy better than ± 3°. The gain setting range is more than 20dB with an accuracy smaller than ± 0.21 dB. The input and output return losses are better than 14 dB for all ports. The gain for transmit and receive is 3 dB. The noise figure for the receive chain is better than 4.5 dB with a third order intercept point of 13.5 dBm.
The P-1dB compression point of the transmit chain is better than 14 dBm. The bias supply voltages are +5 and -5 Volts. The total power consumption of the chip is about 0.3 Watt regardless of the transmit or receive mode. The size of the MFC is 4.2 x 4.2 mm^2.
The integration of functions combined with the low power consumption and the excellent specifications, are making this multi-function chip extremely suitable for future high performance space-based synthetic aperture and phased-array radars.

INTRODUCTION

In phased array radars and synthetic aperture radars (SAR), the demand for circuits with low DC power and small size is growing. Of course the performance and costs of these circuits must be attractive. By using microwave monolithic integrated circuits, these demands can often be met.
Phased array radars use thousands of antennas all driven by transmit/receive modules containing several functions. The space behind the antenna is limited due to the dimensions of the antenna array. It is obvious that the DC power consumption (heat dissipation) and size of each element has to be low. The same applies to space-based SAR where DC power consumption is one of the main demands.

The multi-function X-band MMIC described in this article is designed for application in a space-based SAR. The emphasis lays on integration of several functions while keeping all of the above mentioned demands satisfied. The circuit has to combine phase and amplitude control for transmit/receive and also the necessary switches and amplifiers. The design of the circuit targets at gain over at least a 20% bandwidth at X-band, having good return losses at all ports. The phase and amplitude resolution must be at least 6-bit. By clever distribution of the gain and losses in the designed MMIC and precise modelling of the phase and amplitude control, the overall obtained specifications are impressive. This MMIC is not only very suitable for space-based SAR application but also for phased array radars.

DESIGN TOPOLOGY

The multi-function chip (MFC) consists of an input and output switch for choosing between transmit and receive mode, a low noise amplifier for the receive chain, a common path and a driver amplifier for the transmit chain. The common path of the MFC consists of a 7-bit phase shifter followed by an inter-stage amplifier and a 7 bit attenuator. Figure 1 shows the block diagram of the multi-function chip.

The used circuit topology is based on a trade-off between: noise figure, third-order intercept point, 1dB compression point, insertion gain and power-dissipation. To meet all the MFC requirements, a low-noise amplifier is placed at the input of the receive chain and a driver amplifier is placed at the output of the transmit chain of the chip. So, both amplifiers are placed outside the common path. The amplifier inside the common path is placed between the phase shifter and attenuator to minimise interaction. To minimise power dissipation, the LNA will be switched off in the transmit mode and the driver amplifier will be switched off in the receive mode. In this way only two of the three amplifiers will be used in both modes.

The gain control consists of seven cascaded bits. Each bit consists of a reference path and an attenuation path. The smallest 5 bits are designed using a switched scaled FET configuration. The highest two bits are designed using single-pole double-throw switches to switch between a thru connection and a π attenuator, shown in Gupta et al (1) and Anderson and Joshi (2).
The bit topology of the lowest five bits is depicted in figure 2 (A). This topology consists of two T-attenuators in parallel. The reference path is formed by two series FETs (T1) and one resistor to ground (R1). The attenuation path is formed by two series FETs T2, R2 and T3. To minimise the loss of the reference path, a large series FET (750µm) is selected for T1. The transistor T3 is placed in series with the resistor R2 to increase the cut-off frequency of the attenuator.
For the switched scaled FET attenuator and the switched attenuator, the differential phase error is minimised by inserting line length in one of the attenuation states of each bit. The bit order of the total attenuator is determined by the power handling of each bit in the transmit mode of the MFC.

The seven bit phase shifter consists of six cascaded networks of which one network performs a two bit function. All the used phase networks are of the "embedded switched filter" type. The topology of the 180° phase shifter bit is described by Schindler at al (3). The topologies of the other bits are according to Ayasli et al (4). The total phase shifter is designed to have minimal insertion loss and return loss variation by a proper design of the individual bits. Further improvement of the total phase shifter performance is realised by determining the best bit order with respect to insertion loss and return loss with the power compression behaviour as a constraint. The insertion loss of the total phase shifter is 6.1 ± 0.4 dB.

The layout of the capacitor in combination with the switched FET of the so called "switched series capacitors", figure 2(B), is designed to have minimum series inductance in both states. This highly integrated new layout topology minimises the layout dimensions, insertion loss and allows broadband operation of the phase shifter bits. The layouts of the capacitors that are used in these structures differ from the capacitors that are described in the foundry design manual and are for this reason modelled with Momentum (5).

RESULTS

The results shown in this chapter are the simulation results. For the regular components the standard ED02AH process models supplied by Philips Microwave Limeil, are used for simulation. For the bends, crosses and tee's and some divergent HEMT topologies, TNO-FEL derived their own models. The passive models, like the bends etc., are according to de Hek (6).
The measurement results of the multi-function chip will be available during the conference.

In figure 2, the gain and input/output return losses versus frequency are depicted for the receive mode of the MFC. The traces show the $gain_{max}$ and $gain_{min}$ representing the two outer limits of the gain for all different gain and phase states of the chip. The traces of the input/output return losses are also the maximum values obtained during the different gain and phase states. For the transmit mode of the MFC the same traces are shown in figure 3.
Figure 4 shows the absolute value of the maximum phase error for all different gain and phase states versus frequency. These values are given for the transmit and the receive mode. The same presentation is used for the amplitude error and is given in figure 5 also for transmit and receive mode.

The noise figure versus frequency in receive mode of the MFC is shown in figure 6. The Power output versus frequency at 10 GHz is given in figure 7. The -1dB output compression point is almost 15dBm at 10 GHz. Over the frequency range of 9 to 10 GHz the -1dB compression point is more than 14 dBm.

MANUFACTURING AND CIRCUIT LAYOUT

The multi-function chip is processed at the GaAs foundry of Philips Microwave Limeil with their standard ED02AH process. This process includes 0.2µm enhancement and depletion mode PHEMTs having a unity gain cut-off frequency of 62 GHz, implanted GaAs resistors, MIM capacitors, spiral inductors and via-holes.

The size of the multi-function chip is 4.2 x 4.2 mm^2. Figure 3 shows the layout of the chip.

CONCLUSIONS

The integration of several important functions, like 7-bit phase and amplitude control, low noise amplifier, driver power amplifier and switches for transmit/receive mode, is successfully accomplished.
The integration of functions combined with the low power consumption and the excellent specifications, are making this multi-function chip extremely suitable for future high performance space-based synthetic aperture and phased-array radars.

ACKNOWLEDGEMENT

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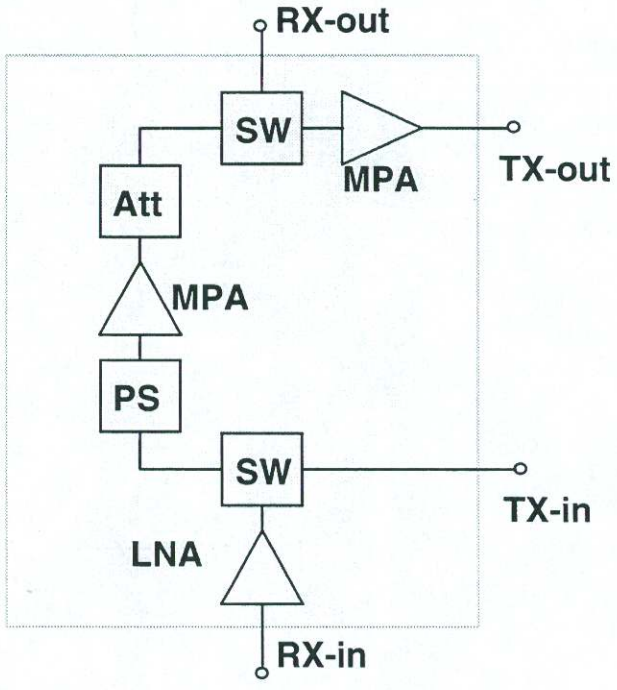

Figure 1: Block diagram of the GaAs multi-function X-band MMIC

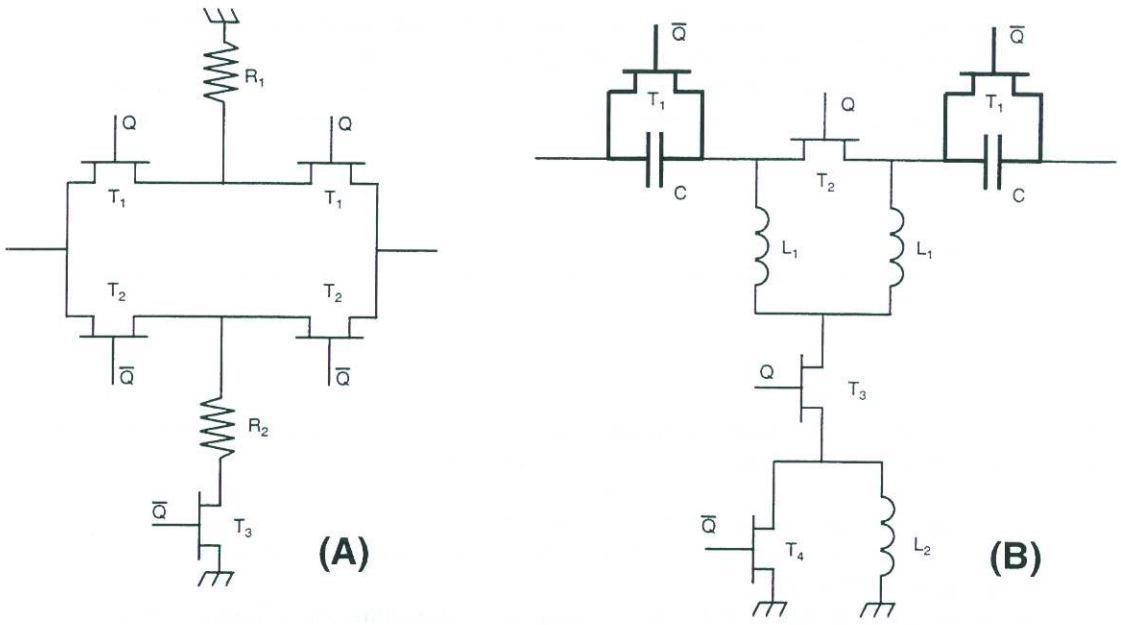

Figure 2: *(A) Block diagram of a switched scaled FET attenuator bit.*
(B) Block diagram of a switched series capacitor used in the phase bits.

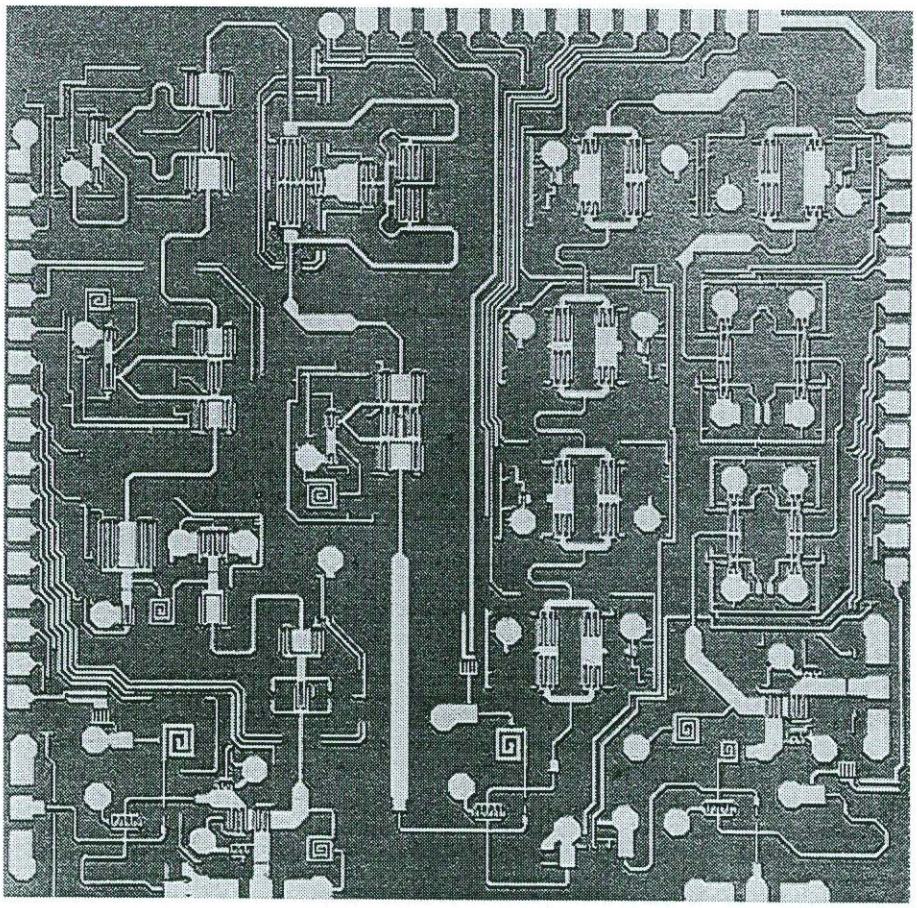

Figure 3: *Lay-out of the GaAs multi-function X-band MMIC (size 4.2 x 4.2 mm^2)*

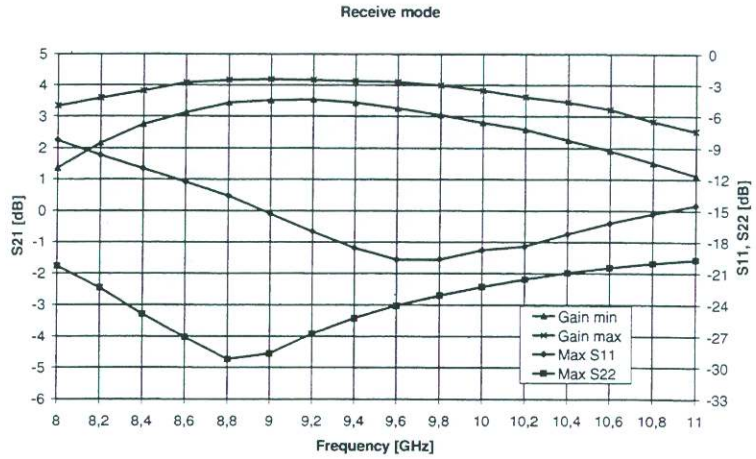

Figure 4: *The gain, input and output return losses versus frequency in receive mode of the MFC. The values are the maximum (or minimum) obtained over all different amplitude and phase states.*

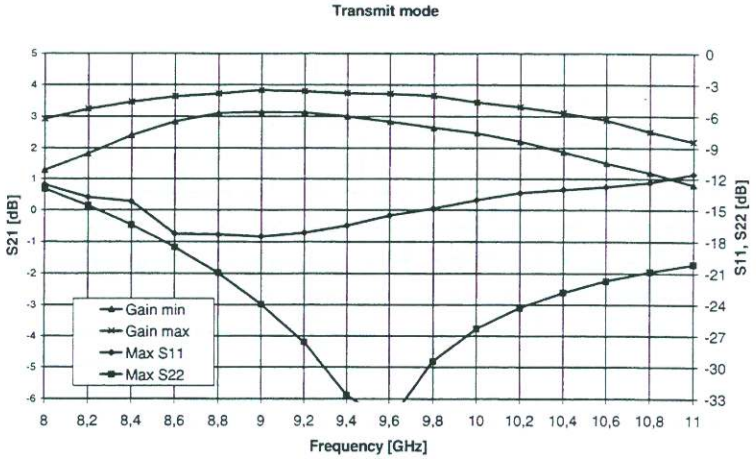

Figure 5: *The gain, input and output return losses versus frequency in transmit mode of the MFC. The values are the maximum (or minimum) obtained over all different amplitude and phase states.*

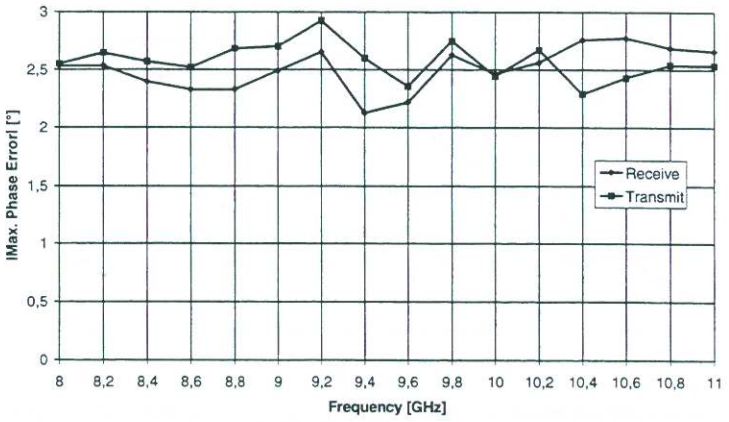

Figure 6: *The absolute value of the maximum phase error versus frequency in transmit and receive mode of the MFC. The values are obtained over all different amplitude and phase states.*

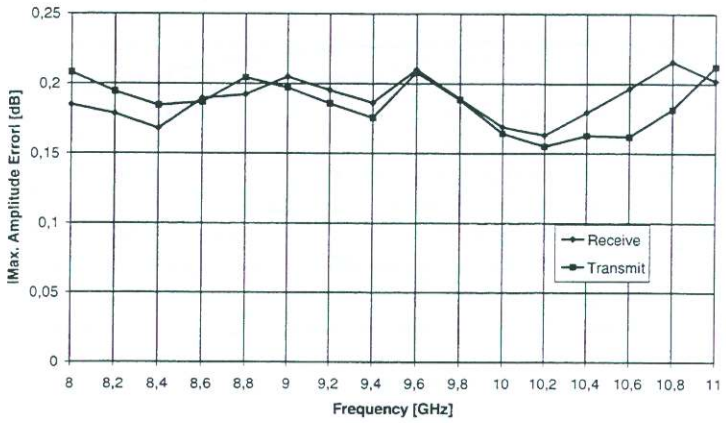

Figure 7: *The absolute value of the maximum amplitude error versus frequency in transmit and receive mode of the MFC. The values are obtained over all different amplitude and phase states.*

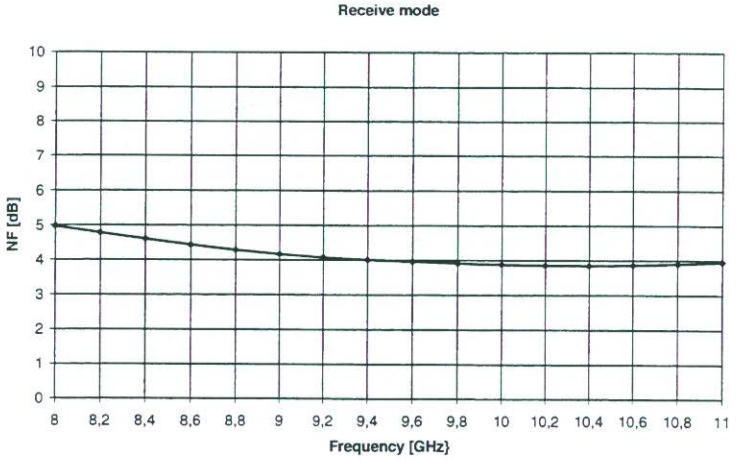

Figure 8: *The noise figure versus frequency in receive mode of the MFC.*

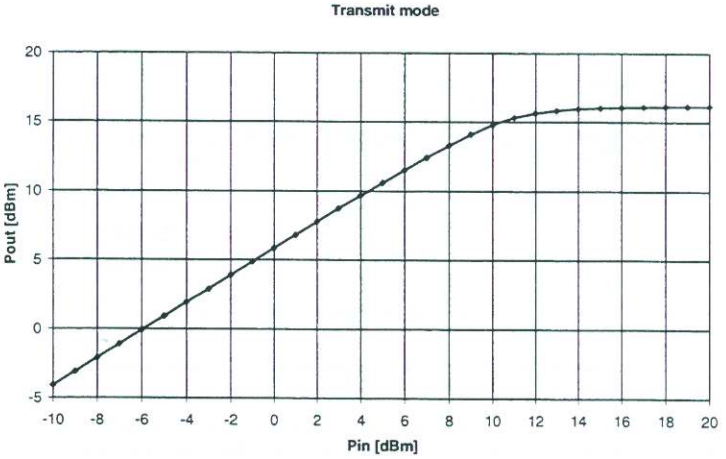

Figure 9: *The power output versus input power in transmit mode of the MFC at 10 GHz. The -1dB compression point at this frequency is almost 15dBm.*